REMARKS

Claims 1 and 5-8 are currently pending. By this Amendment, claims 1 and 6 are amended and claims 2-4 are cancelled. No new matter is added. Reconsideration in view of the above-outlined amendments and the following remarks is respectfully requested.

Claims 1-8 were rejected under 35 USC § 102(b) under U.S. Patent No. 6,387,821 to Aoki. This rejection is respectfully traversed.

Aoki discloses a method of manufacturing a semiconductor device having a multi-layer interconnection connecting an upper wiring and a metal wiring made of a copper type metal material through a via hole. The semiconductor device has damascene interconnections forming the lower wiring and the upper wiring. Aoki forms the lower wiring on a semiconductor substrate by first forming a silicon oxide film 101 and then an HSQ film 102 on the substrate. A photoresist mask 103 having a predetermined pattern is formed then dry etched to form a groove in the HSQ film 102 for buried lower wiring. A TiN film 104 is applied as a barrier metal film. A copper film 105 is then sputtered to fill the groove. After the completion of the lower wiring, a HSQ layer is formed and heat treated at 150 C°, 200 C° and 350 C°. The HSQ layer is further heat treated at 400 C° in a nitrogen atmosphere for 60 minutes to form a HSQ film 106. A resist mask 107 having a pattern for via holes is then formed on the HSQ film. Dry etching is then performed to form part of a via hole in the HSQ film 106. The dry etching is stopped before the bottom of the via hole reaches the copper film 105. A resist mask 108 is then formed on the HSQ film 106. Dry etching is performed using this resist mask 108 to form a hole having a T-shaped section in the HSQ film 106. A TiN film 109 is then sputtered as a barrier metal film followed by a copper film 111 to fill the hole having a T-shaped section.

By contrast, amended claim 1 is directed to a method of forming metal wiring in a semiconductor device. The method includes forming a bottom metal pattern on a semiconductor substrate. A low temperature oxide is formed as an insulating layer on the semiconductor substrate including the bottom metal pattern. Aoki does not disclose the use of a low temperature oxide as the insulating layer. Instead, Aoki discloses the use of an HSC film. The claimed low temperature oxide is formed at the temperature of 150~500 C°. Aoki also does not disclose this feature. Instead, Aoki deposits the HSC film then performs a stepped heat treating process (i.e., 150 C°, 200 C° and 350 C°) followed by an additional heat treatment step. A first photoresist pattern is formed for forming via hole on the low temperature oxide. An unfinished via hole is then formed by selectively removing the low temperature oxide for a prescribed thickness using the first photoresist pattern as a mask. The

thickness of the low temperature oxide remaining inside the via hole is equal to or less than a thickness of an upper part of a damascene contact. This feature is not disclosed or suggested by Aoki. Instead, Aoki dry etches the HSQ film to form part of the via hole. The dry etching is stopped before the via hole reaches the copper film 105. Aoki does not disclose, teach or suggest that the thickness of the low temperature oxide remaining inside the via hole is equal to or less than a thickness of an upper part of a damascene contact. The first photoresist pattern is then removed. A second photoresist pattern is then formed for forming a damascene pattern on the low temperature oxide around the unfinished via hole. A damascene pattern is then formed by selectively removing the low temperature oxide using the second photoresist pattern as a mask. The second photoresist pattern is then removed. A metal wiring via damascene contact is then formed by filling metal in the damascene pattern.

Applicant respectfully submits that Aoki does not disclose, teach or suggest the subject matter of amended claim 1. Claim 1 is allowable over Aoki. Claims 5-8 depend from claim 1 and are allowable over Aoki for at least the same reasons. Reconsideration and withdrawal of the rejection are respectfully requested.

Applicant respectfully submit that the claims define subject matter that is patentable over the prior art cited of record. It is respectfully submitted that the application is in condition for allowance. Should further issues require resolution prior to allowance, the Examiner is requested to telephone applicant's undersigned attorney at the number below. Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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